Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (canceled)

Claim 2. (previously presented) A method for aligning an input clock signal with a delay clock signal, the method comprising:

detecting phases of the input clock signal and the delay clock signal to generate a phase detection signal by dividing a frequency of the delay clock signal using a first frequency divider to generate a first frequency divided delay signal~~;~~, and comparing phases of the input clock signal with the first frequency divided delay signal to generate the phase detection signal using a phase comparator;

detecting edges of the delay clock signal to generate a detect signal;

selecting the delay clock signal or the input clock signal to provide a selection signal in response to the detect signal; and

controlling a delay of the selection signal in response to the phase detection signal to generate the delay clock signal.

Claim 3. (original) The method of claim 2 further comprising:

dividing the frequency of the delay clock signal using a second frequency divider to generate an output clock signal.

Claim 4. (original) The method of claim 3 further comprising:

providing the output clock signal to programmable circuit elements in a programmable integrated circuit.

Claim 5. (previously presented) A method for aligning an input clock signal with a delay clock signal, the method comprising:

detecting phases of the input clock signal and the delay clock signal to generate a phase detection signal;

detecting edges of the delay clock signal to generate a detect signal;

selecting the delay clock signal or the input clock signal to provide a selection signal in response to the detect signal; and

controlling a delay of the selection signal in response to the phase detection signal to generate the delay clock signal, wherein selecting the delay clock signal or the input clock signal to provide the selection signal in response to the detect signal further comprises:

coupling a feedback loop around an adjustable delay circuit to form an oscillator circuit that generates the delay clock signal when the detect signal has a first value that selects the delay clock signal as the selection signal; and

decoupling the feedback loop from an input of the adjustable delay circuit when the detect signal has a second value that selects the input clock signal as the selection signal.

Claim 6. (previously presented) The method of claim 5 wherein controlling the delay of the selection signal in response to the phase detection signal to generate the delay clock signal further comprises:

increasing the delay of the selection signal through an adjustable delay circuit when the phase detection signal indicates that an edge of the delay signal is ahead of a corresponding edge of the input signal; and

decreasing the delay of the selection signal through the adjustable delay circuit when the phase detection signal indicates that an edge of the delay signal is behind a corresponding edge of the input signal.

Claim 7. (previously presented) The method of claim 2 wherein selecting the delay clock signal or the input clock signal to provide the selection signal in response to the detect signal further comprises:

selecting the delay clock signal as the selection signal regardless of the value of the detect signal when a disable signal has a predefined value.

Claim 8. (canceled)

Claim 9. (previously presented) A circuit for aligning a periodic input signal with a delay signal, the circuit comprising:

a phase detector having a first input coupled to the periodic input signal;

an adjustable delay circuit coupled to an output of the phase detector that generates the delay signal at an output of the adjustable delay circuit;

a feedback loop circuit coupled to the output of the adjustable delay circuit;

an edge detector circuit having an input coupled to the output of the adjustable delay circuit;

a multiplexer having data inputs coupled to the feedback loop and the periodic input signal, a select input coupled to receive a detect signal from the edge detector circuit, and an output coupled to an input of the adjustable delay circuit; and

a first frequency divider circuit having an input coupled to the output of the adjustable delay circuit and an output coupled to a second input of the phase detector, the first frequency divider dividing a frequency of the delay signal by N to generate a divided signal.

Claim 10. (original) The circuit according to claim 9 wherein the edge detector circuit generates a HIGH pulse one-half a period of the delay signal before a rising edge of the divided signal.

Claim 11. (original) The circuit according to claim 9 wherein the first frequency divider is a counter circuit, and the edge detector circuit generates a HIGH pulse after the counter circuit counts a predetermined number of edges of the delay signal.

Claim 12. (previously presented) The circuit according to claim 9 further comprising:

a second frequency divider circuit having an input coupled to the output of the adjustable delay circuit that generates a periodic output signal, wherein the second frequency divider divides a frequency of the delay signal by M, and the periodic output signal has a frequency that is N/M times the frequency of the input signal.

Claim 13. (previously presented) The circuit according to claim 9 further comprising:

a logic gate coupled to the select input of the multiplexer, to an output of the edge detector circuit, and to a memory cell.

Claim 14. (previously presented) The circuit according to claim 13 wherein the adjustable delay circuit comprises an odd number of inverting buffers coupled together in series.

Claim 15. (previously presented) The circuit according to claim 13 wherein:

the feedback loop is coupled to the input of the adjustable delay circuit when the detect signal is in a first state, and the input of the adjustable delay circuit receives the periodic input signal when the detect signal is in a second state,

the edge-detector circuit causing the detect signal to transition from the first state to the second state, and causing the detect signal to transition from the second state to the first state after one period of the delay signal.

Claim 16. (canceled)

Claim 17. (previously presented) A circuit for aligning an input clock signal with a delay signal, the circuit comprising:

means for detecting a phase difference between the input clock signal and the delay signal to generate a phase difference signal;

means for controlling a phase of the delay signal in response to the phase difference signal;

means for detecting edges of the delay signal to generate a detect signal;

means for selecting the input clock signal or the delay signal as a selected signal in response to a value of the detect signal, wherein the selected signal is delayed by the means for controlling to generate the delay signal; and

means for dividing a frequency of the delay signal by N to generate a first divided signal, wherein the means for detecting the phase difference between the input clock signal and the delay signal compares the input clock signal to the first divided signal.

Claim 18. (original) The circuit defined in claim 17 further comprising:

means for dividing the frequency of the delay signal by M to generate an output clock signal, wherein a frequency of the output clock signal is N/M times the frequency of the input clock signal.

Claim 19. (previously presented) The circuit defined in claim 17 further comprising:

means for causing the means for selecting to select the delay signal as the selected signal regardless of the value of the detect signal when a disable signal is a predetermined value.

Claim 20. (previously presented) The circuit defined in claim 17 wherein the means for detecting the edges of the delay signal counts falling edges of the delay signal.

Claim 21. (previously presented) The circuit defined in claim 17 wherein the means for selecting selects the delay signal as the selected signal during a first state of operation, and the means for selecting selects the input clock signal as the selected signal for one period of the delay signal during a second state of operation.

Claim 22. (previously presented) The circuit defined in claim 21 wherein the circuit for aligning the input clock signal with the delay signal in part of a field programmable gate array.

Claim 23. (canceled)

Claim 24. (currently amended) ~~The circuit defined in claim 23 further comprising:~~

A circuit that is a hybrid of a phase-locked loop (PLL) and a delay locked loop (DLL), the circuit comprising:

a phase detector circuit that receives an input clock signal;

an adjustable delay circuit coupled to receive an output of the phase detector circuit, the adjustable delay circuit generating a delay signal; and

a selector that selects the delay signal as a selected signal during a first state of operation to cause the circuit to operate as a PLL, and wherein the selector selects the input clock signal as the selected signal during a second state of operation to cause the circuit to operate as a DLL;

a first frequency divider coupled to receive the delay signal and coupled to transmit a divided signal to an input of the phase detector.

Claim 25. (previously presented) The circuit defined in claim 24 further comprising:

a second frequency divider circuit coupled to receive the delay signal.

Claim 26. (previously presented) The circuit defined in claim 24 wherein the frequency divider is a counter circuit.

Claim 27. (currently amended) ~~The circuit defined in claim 23 further comprising:~~ A circuit that is a hybrid of a phase-locked loop (PLL) and a delay locked loop (DLL), the circuit comprising:

a phase detector circuit that receives an input clock signal;

an adjustable delay circuit coupled to receive an output of the phase detector circuit, the adjustable delay circuit generating a delay signal;

a selector that selects the delay signal as a selected signal during a first state of operation to cause the circuit to operate as a PLL, and wherein the selector selects the input clock signal as the selected signal during a second state of operation to cause the circuit to operate as a DLL; and

a logic gate coupled to a select input of the selector and coupled to receive a signal that causes the circuit to remain in the first state of operation.